

FIG. 1  
PRIOR ART

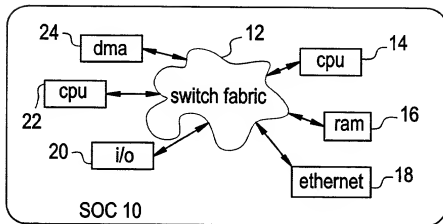


FIG. 2

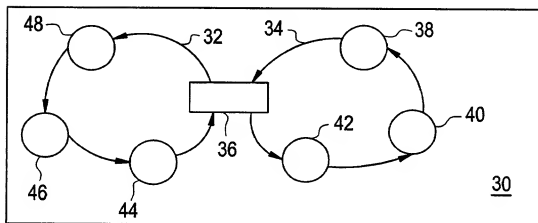


FIG. 3

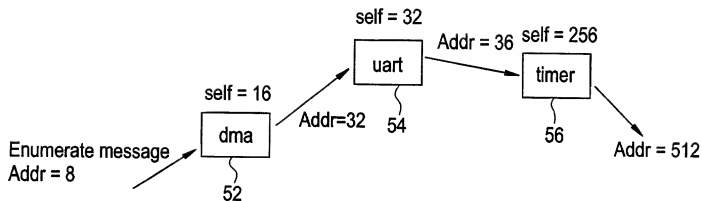


FIG. 4

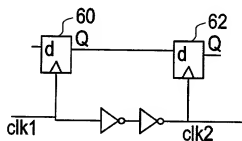


FIG. 5

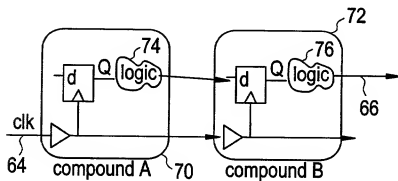


FIG. 6

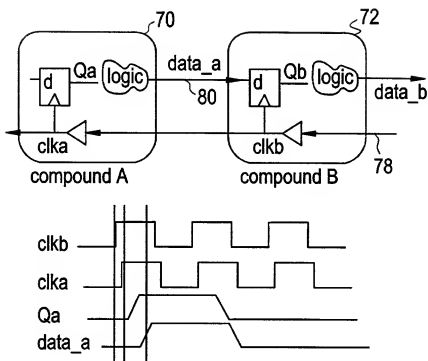


FIG. 7

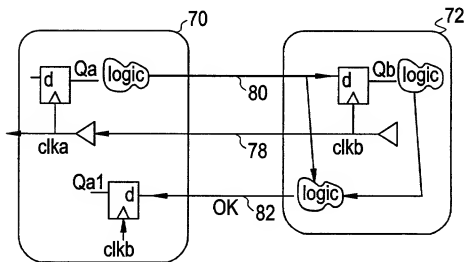


FIG. 8

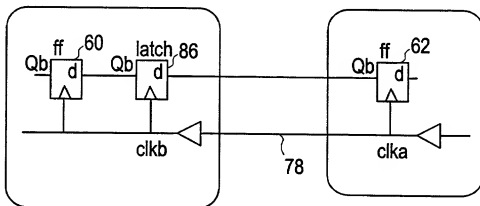
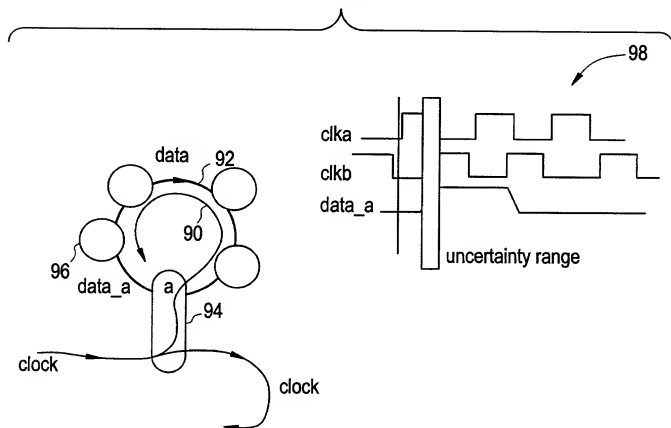


FIG. 9



10061326.092402

FIG. 10

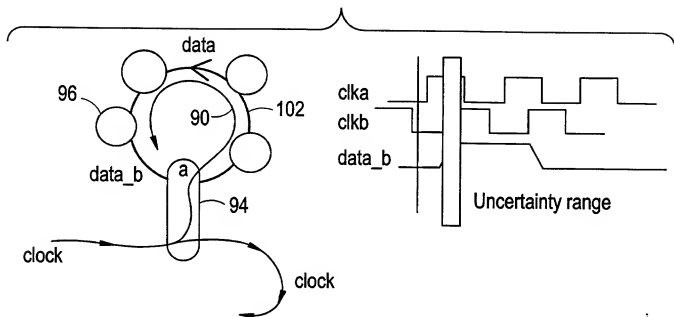


FIG. 11

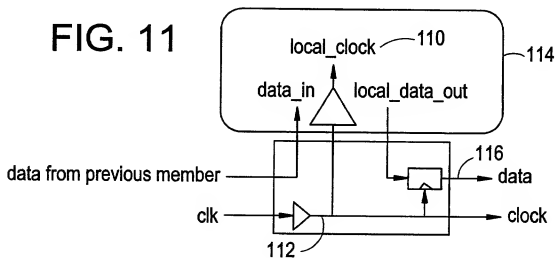


FIG. 12

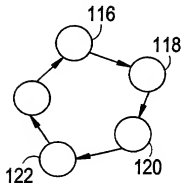


FIG. 13

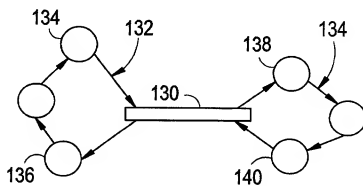


FIG. 14

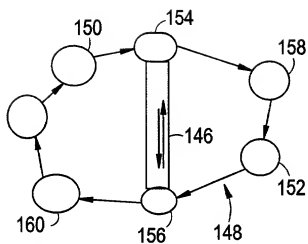


FIG. 15

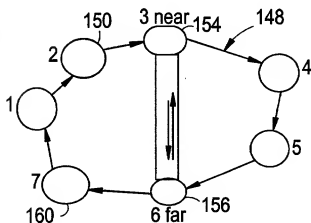


FIG. 16

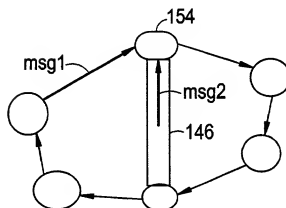


FIG. 17

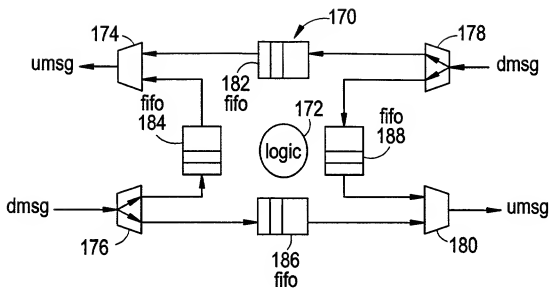


FIG. 18

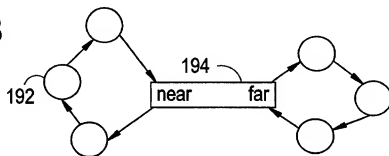


FIG. 19

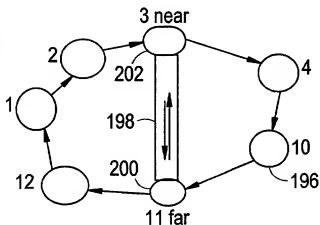


FIG. 20

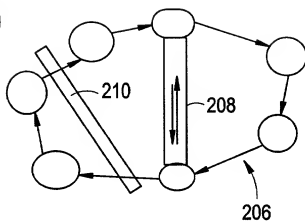


FIG. 21

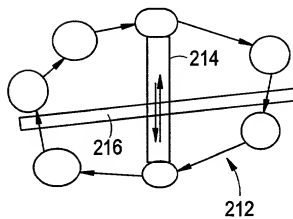


FIG. 22

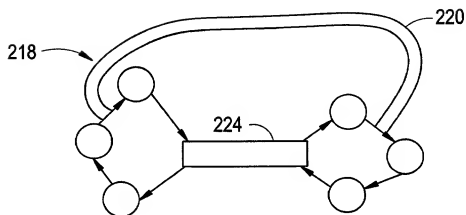




FIG. 23

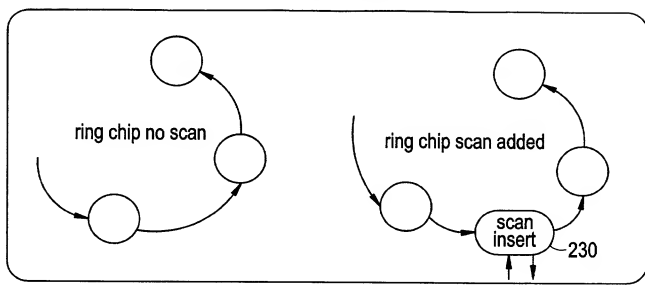


FIG. 24

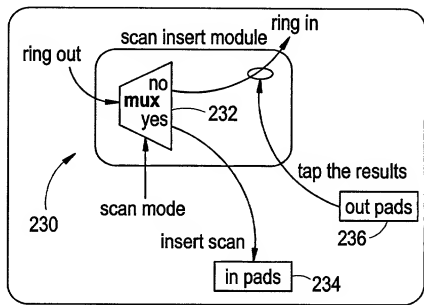


FIG. 25

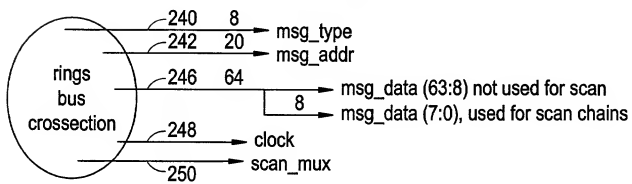


FIG. 26

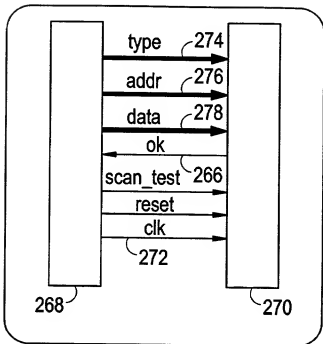


FIG. 27

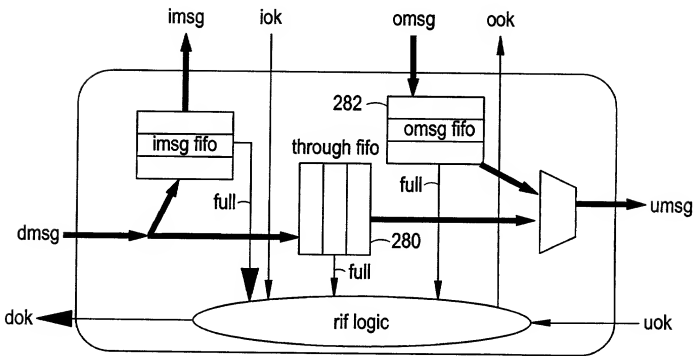


FIG. 28

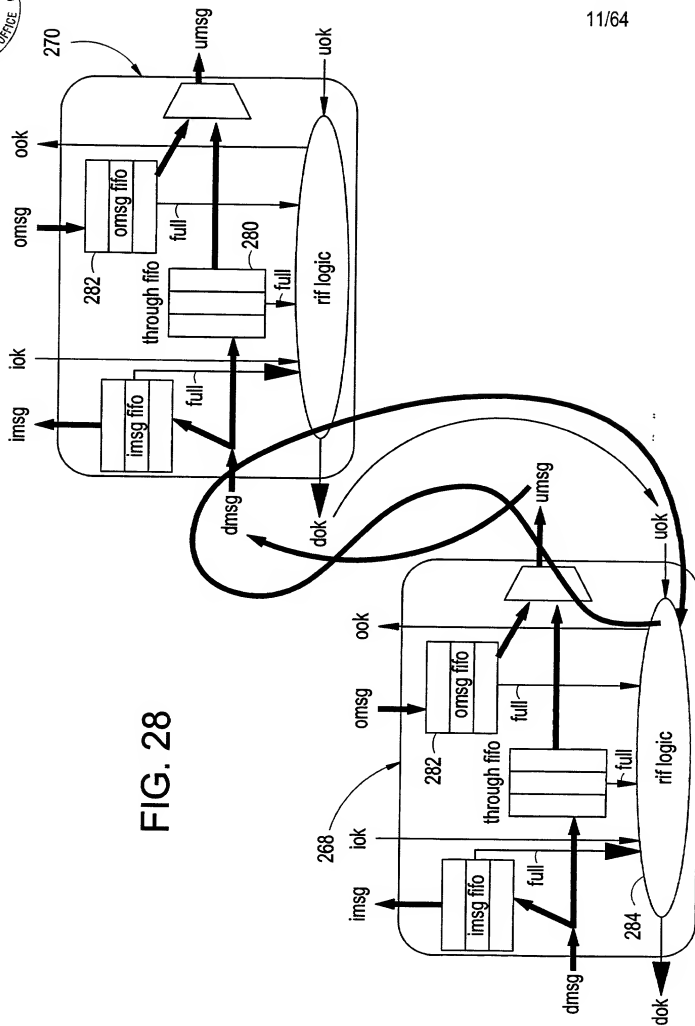


FIG. 29

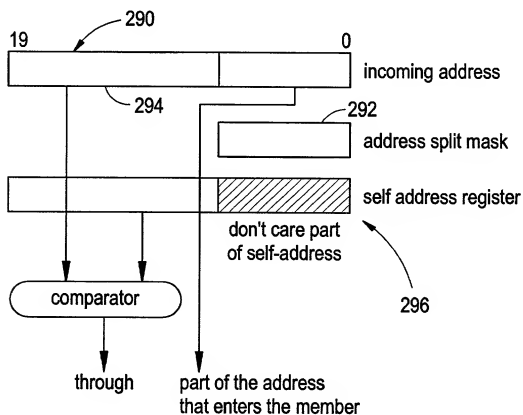


FIG. 30

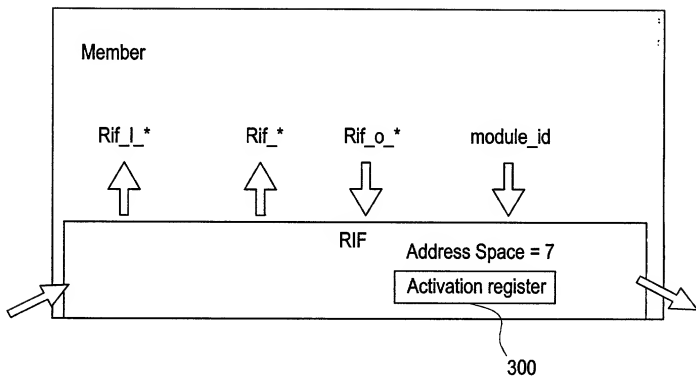


FIG. 31

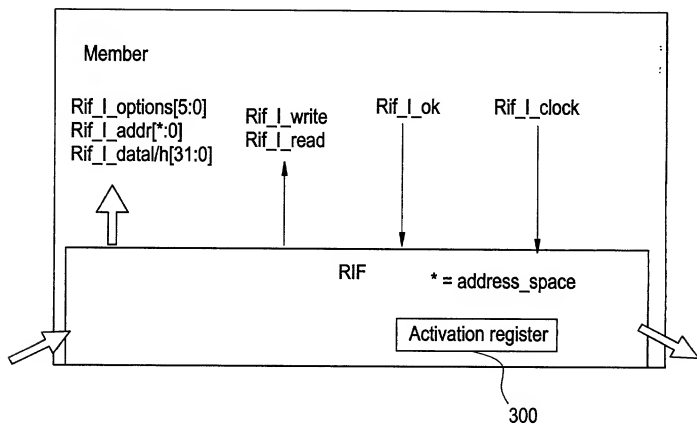


FIG. 32

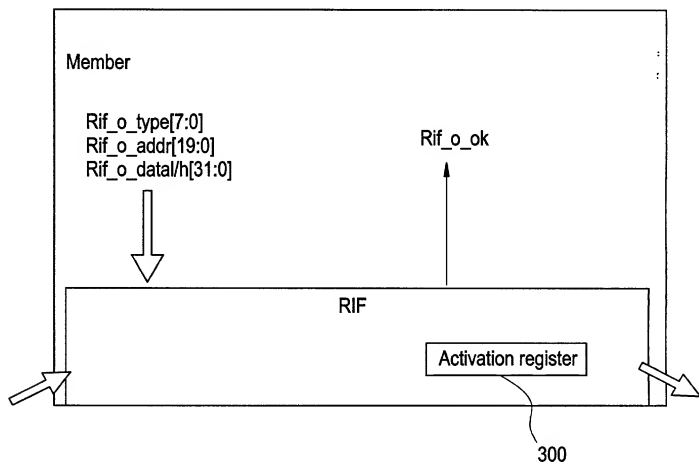


FIG. 33

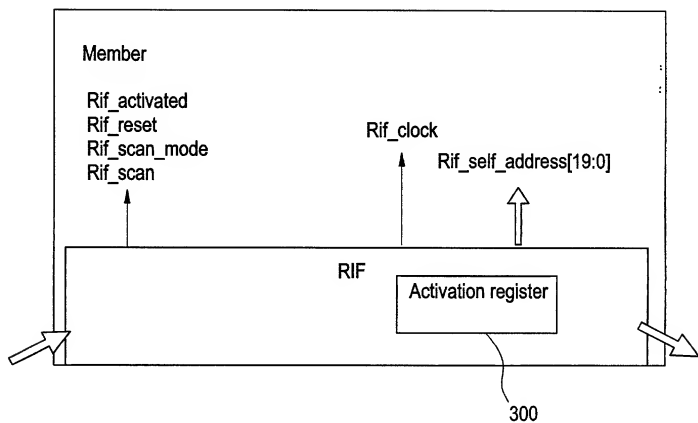




FIG. 34

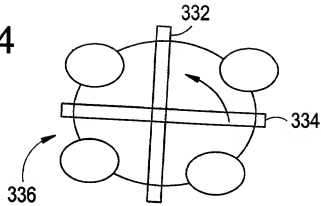


FIG. 35

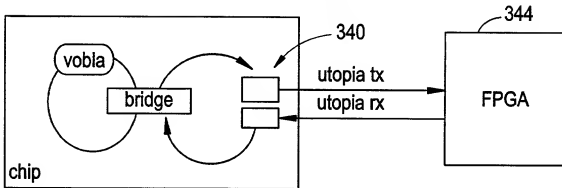
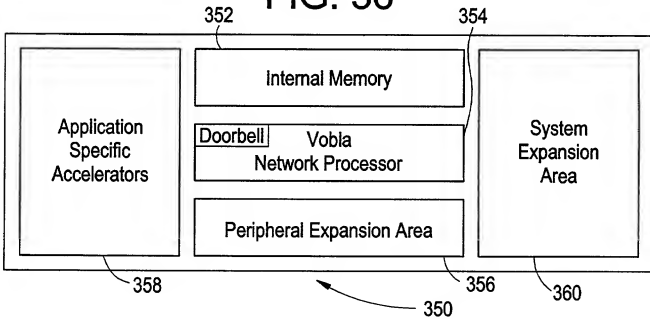
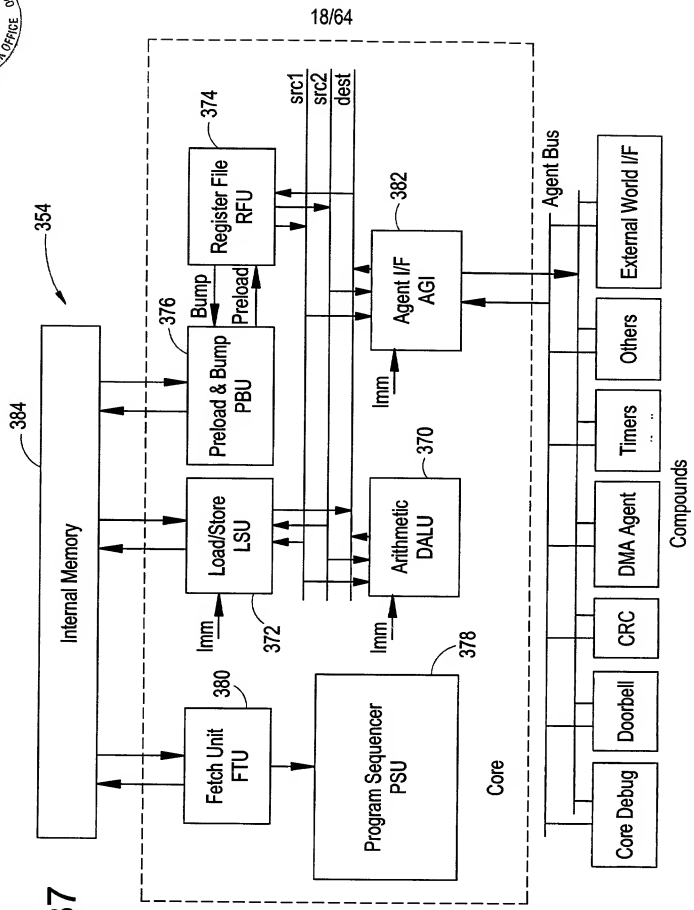


FIG. 36



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FIG. 37



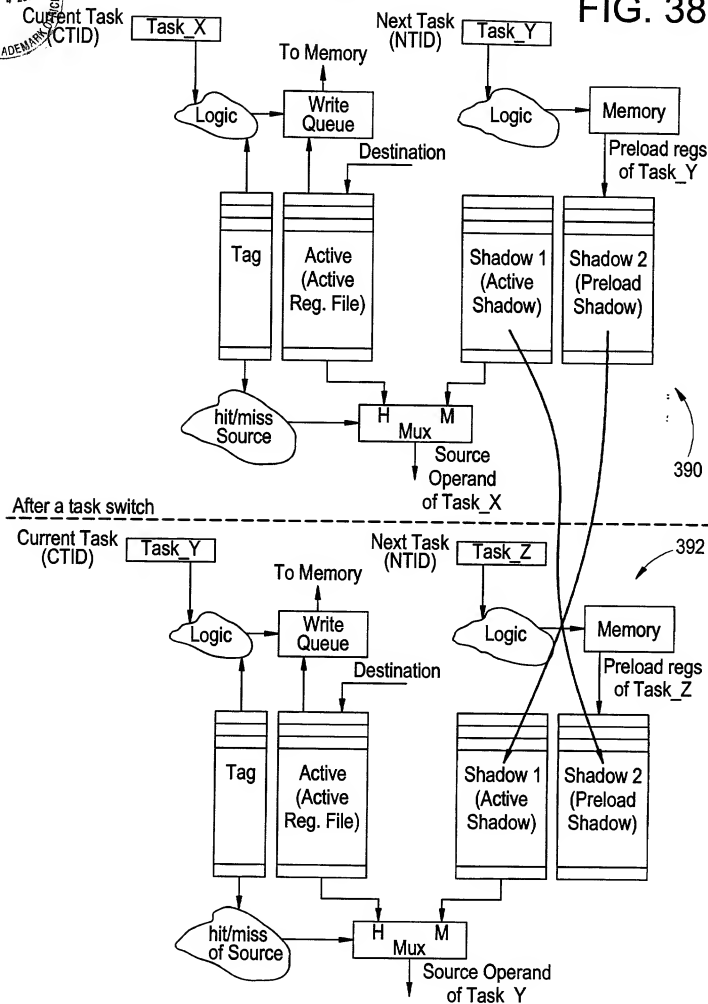


FIG. 39

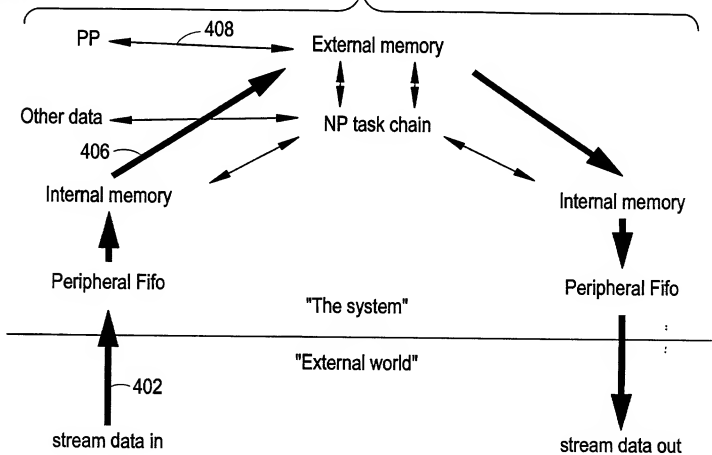


FIG. 40

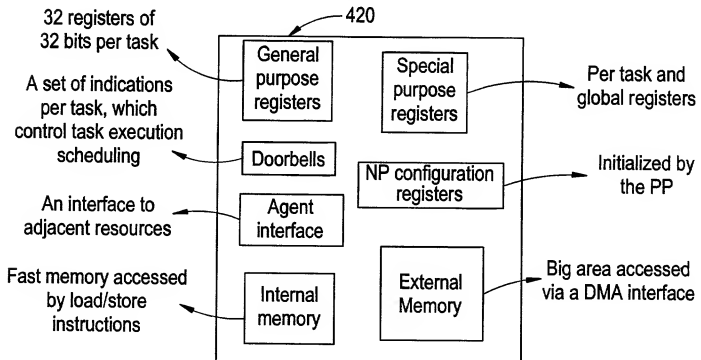


FIG. 41

R1 register

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0



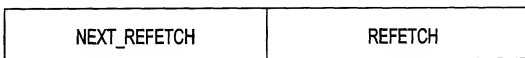
s - sticky bit  
 eq - equal/zero  
 lt - less then/negative  
 gt - greater then/positive  
 c - carry  
 mb - reflection of the RAM mult-reader busy indication

430

FIG. 42

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

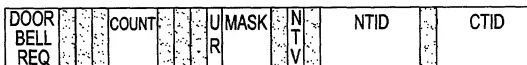
REFETCH SPR  
(spr index - 0)



440

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

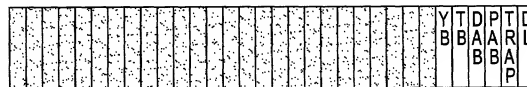
TASK SPR  
(spr index - 1)



442

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

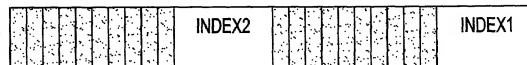
TRAP SPR  
(spr index - 2)



444

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

MINDEX SPR  
(spr index - 3)



446

FIG. 43

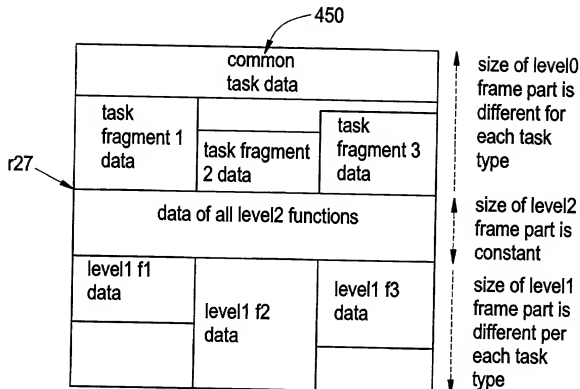


FIG. 44

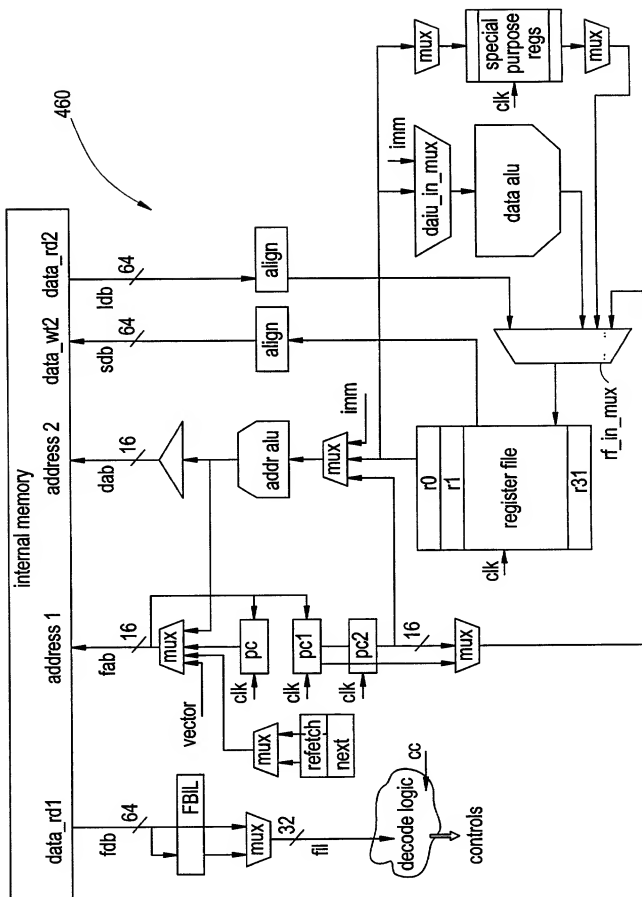
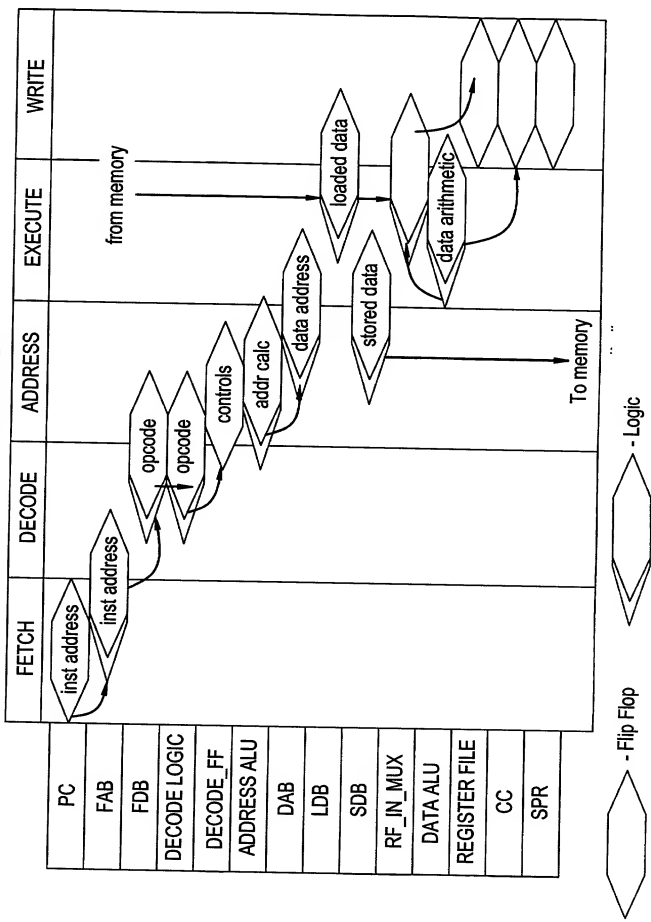


FIG. 45



480



FIG. 46

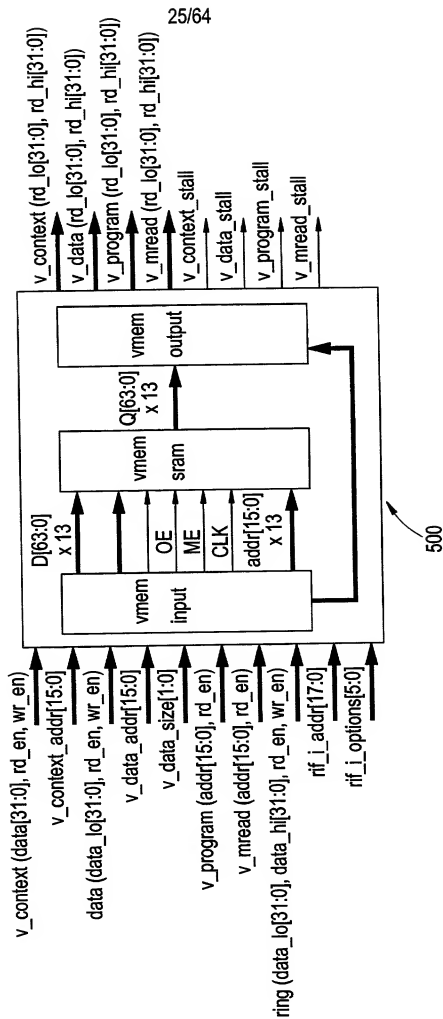


FIG. 47

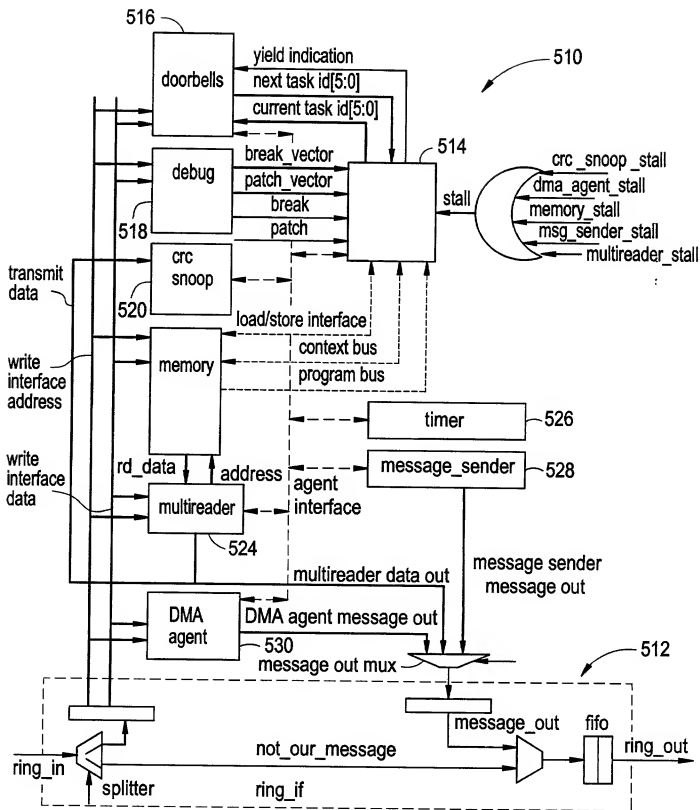


FIG. 48

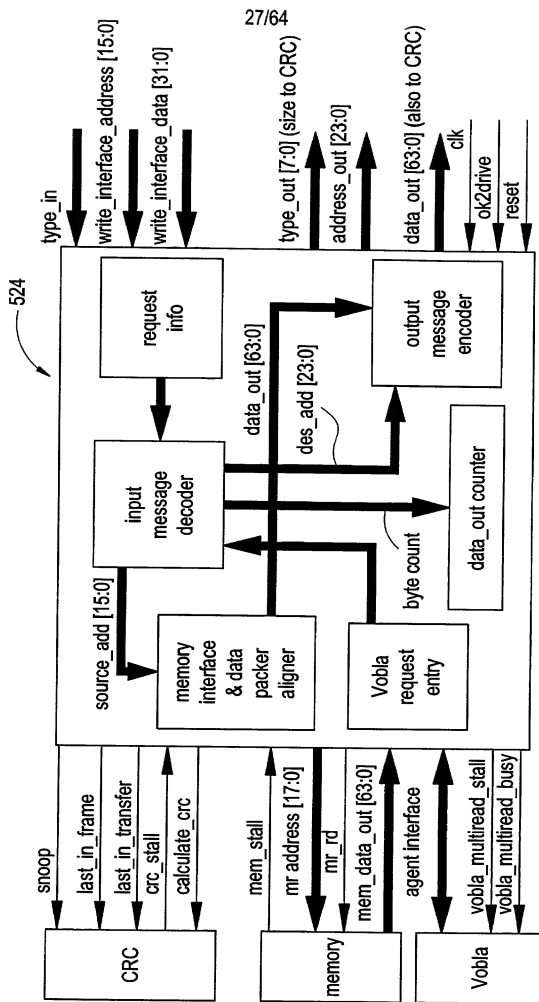
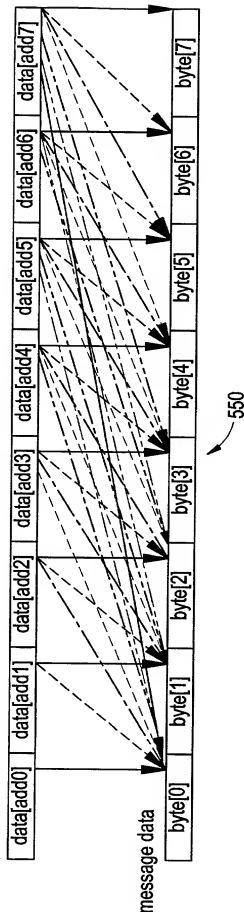


FIG. 49

memory data



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FIG. 50

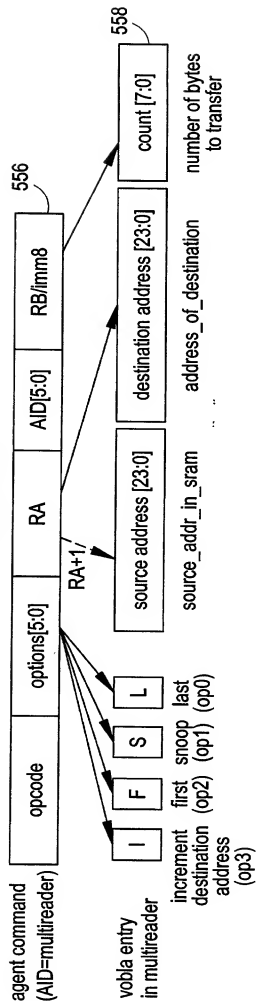


FIG. 51

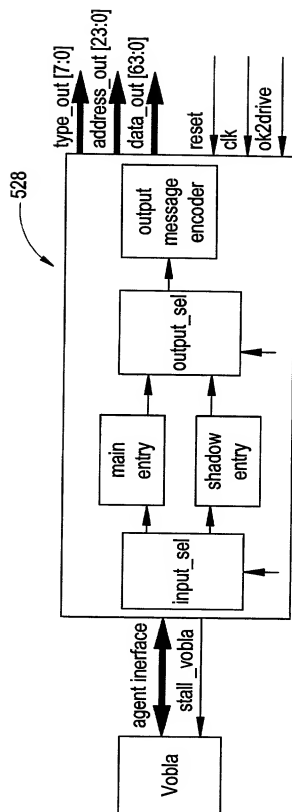


FIG. 52

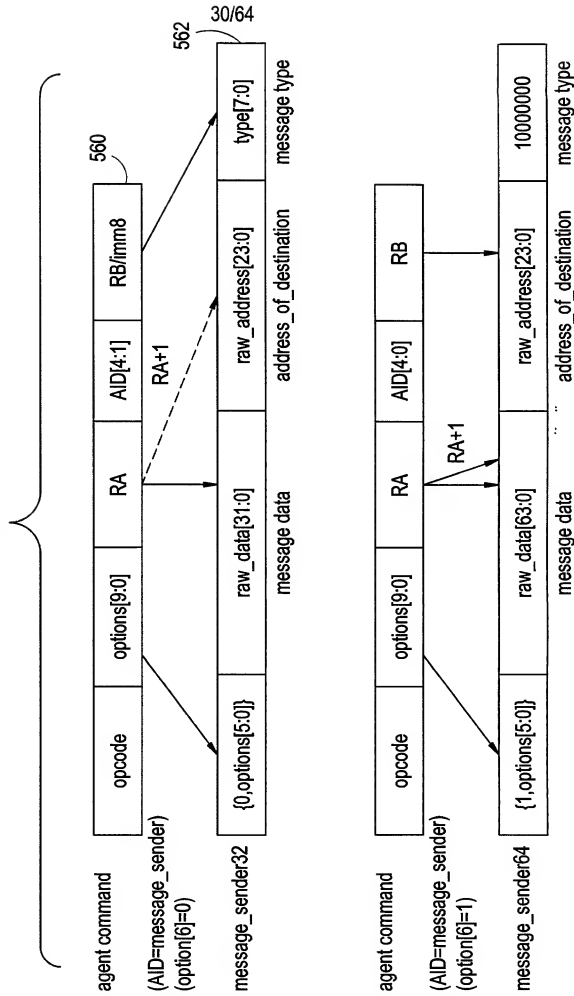


FIG. 53

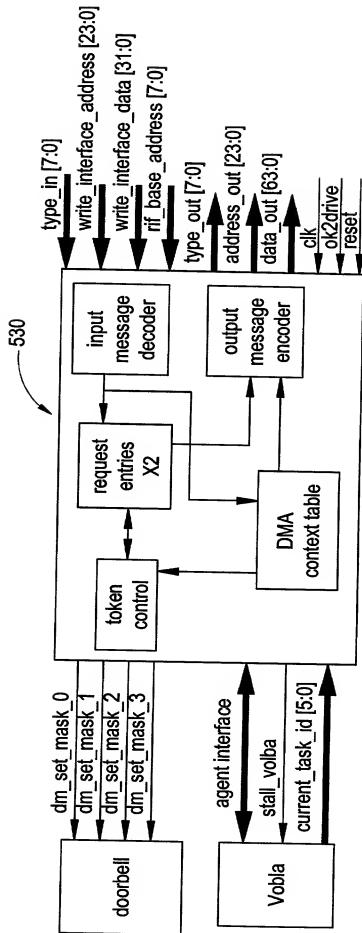


FIG. 54

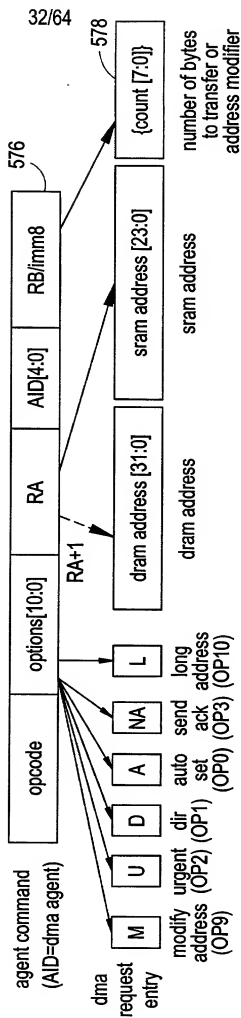




FIG. 55

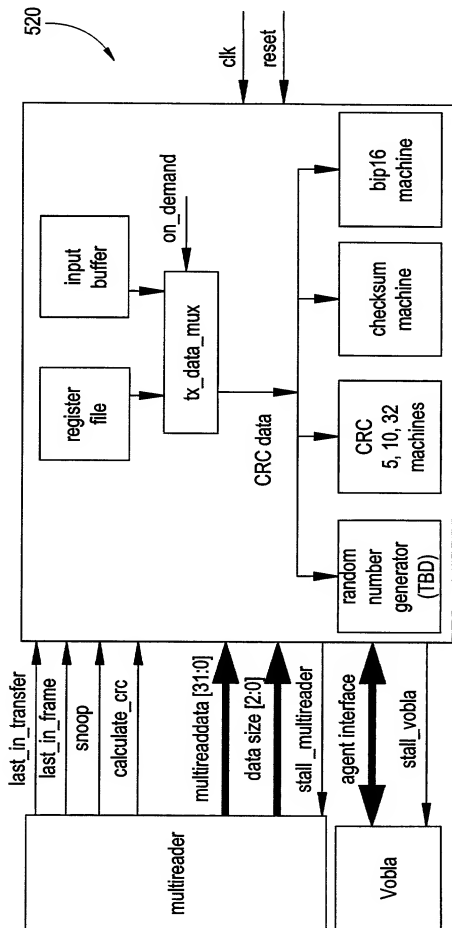


FIG. 56

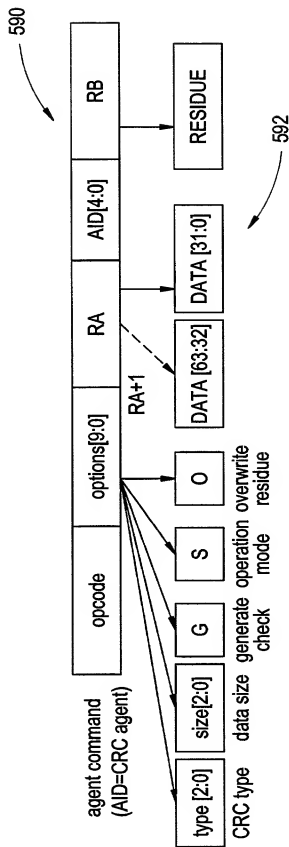


FIG. 57

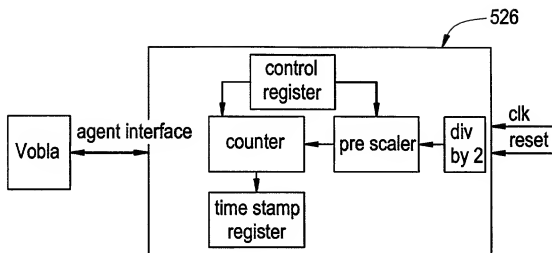


FIG. 58

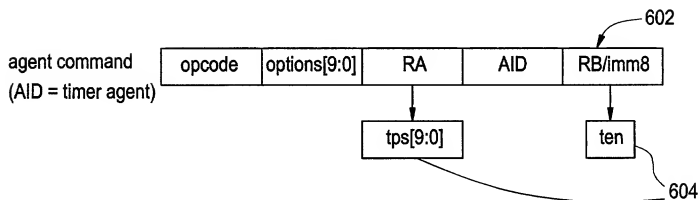


FIG. 59

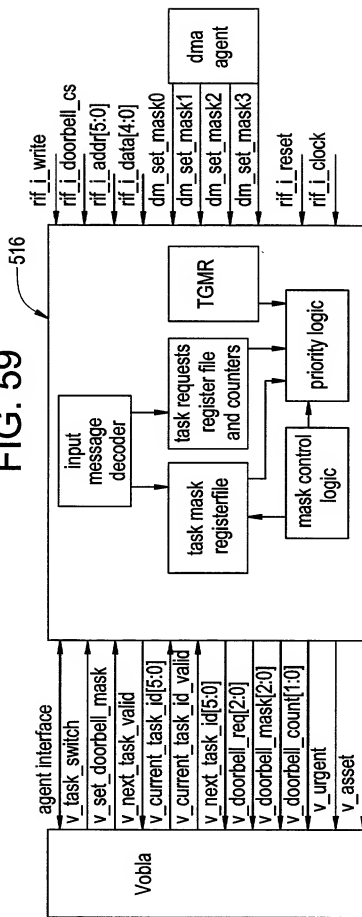


FIG. 60

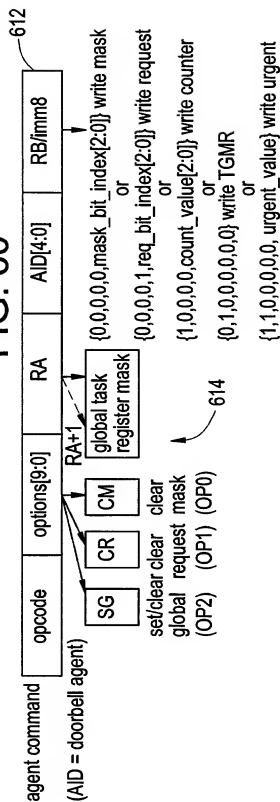


FIG. 61

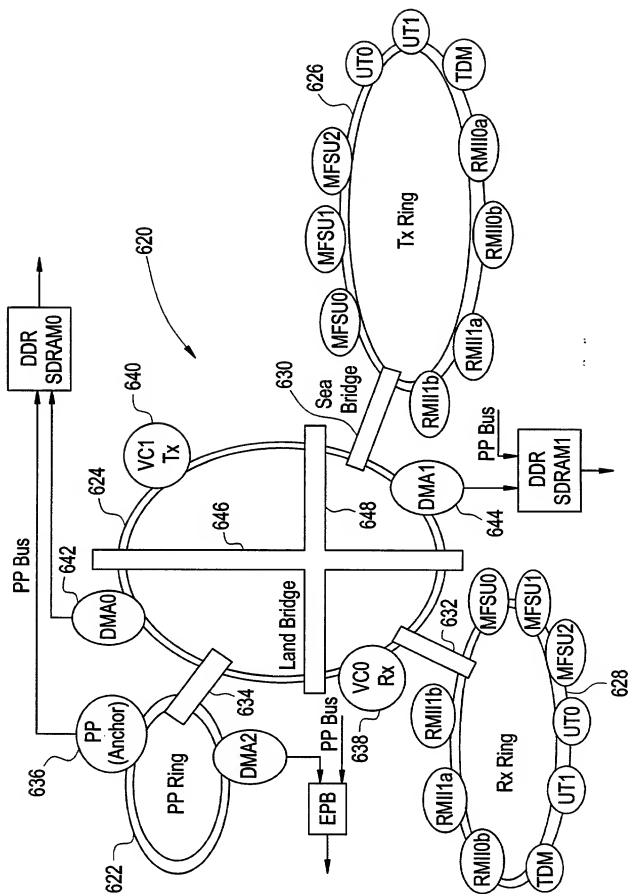
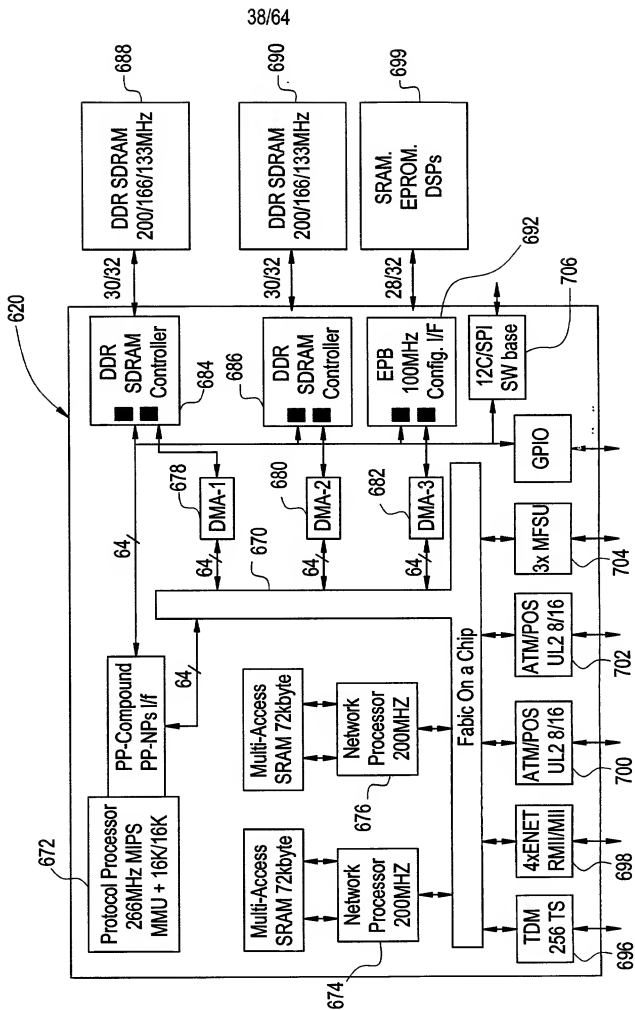


FIG. 62



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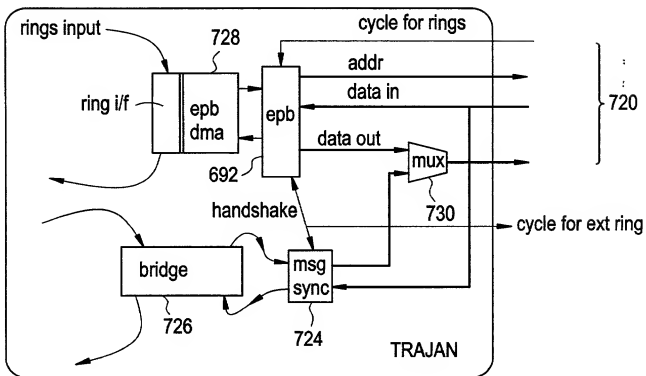
[illegible]

FIG. 64

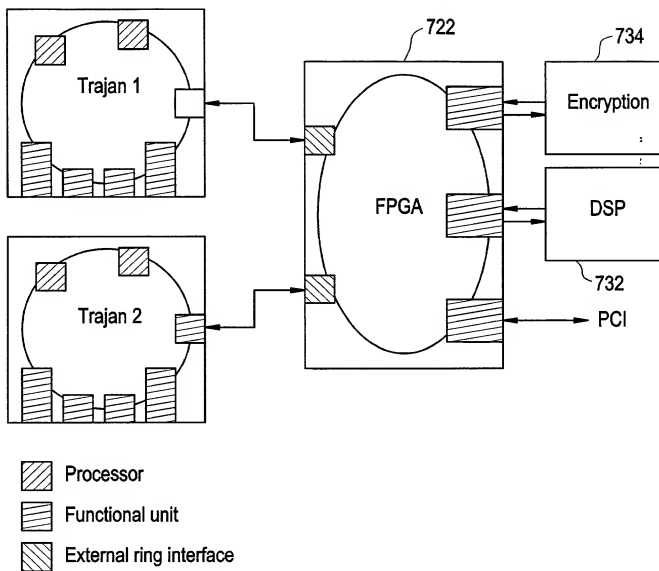




FIG. 65

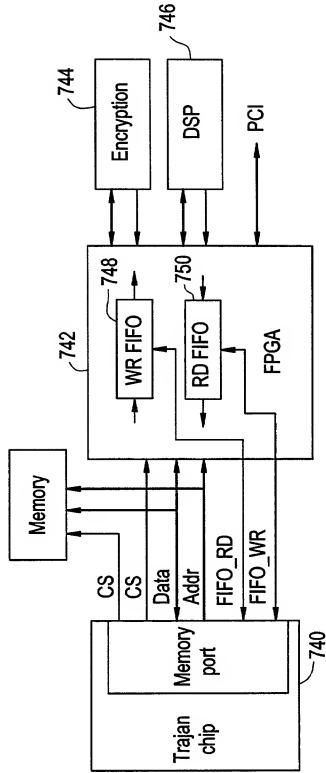


FIG. 66

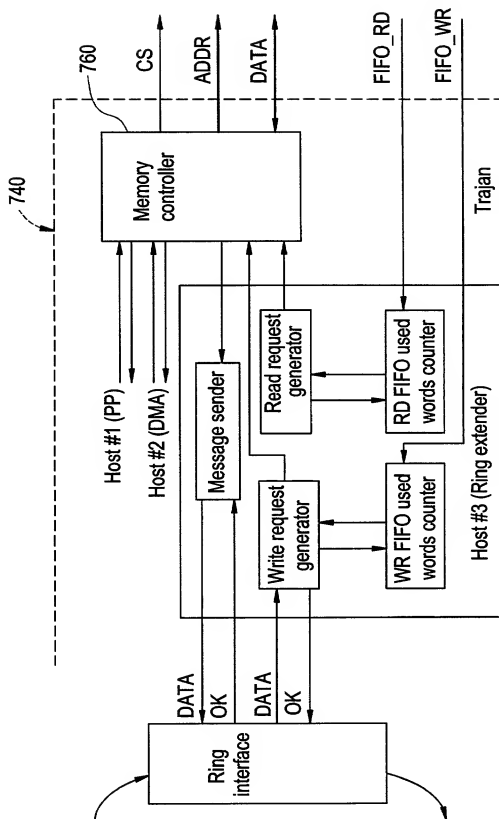


FIG. 67

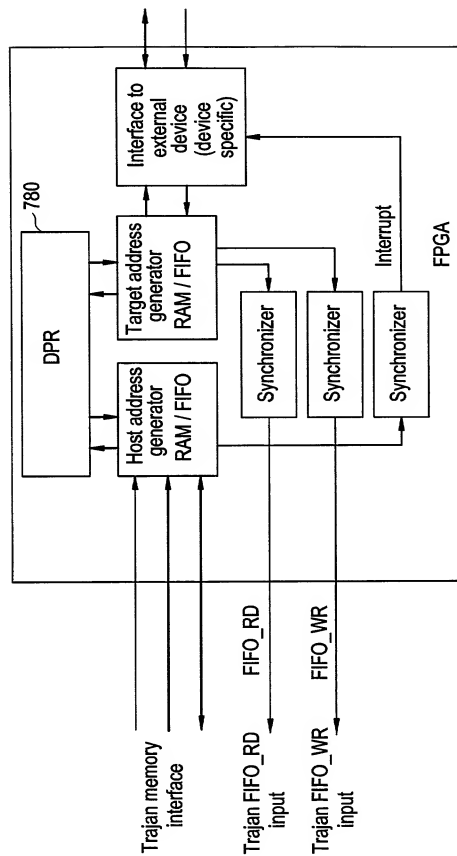


FIG. 68

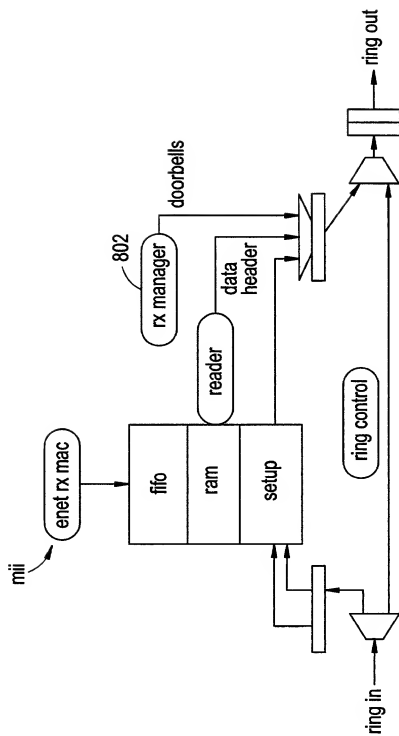


FIG. 69

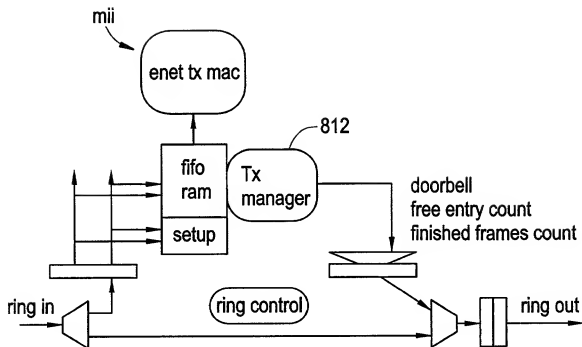
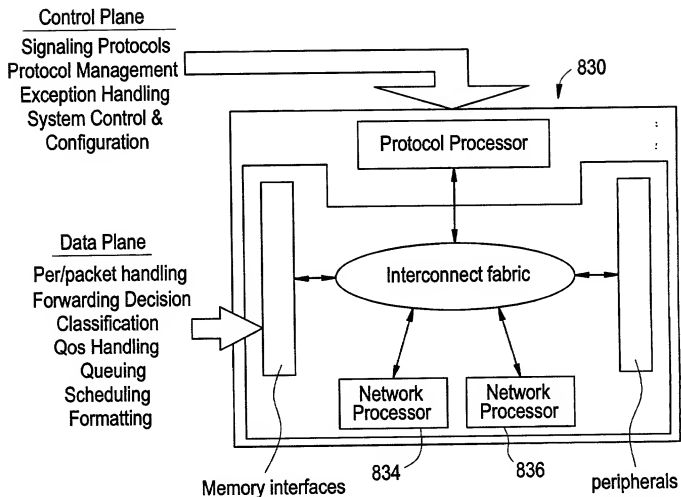


FIG. 70



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FIG. 71

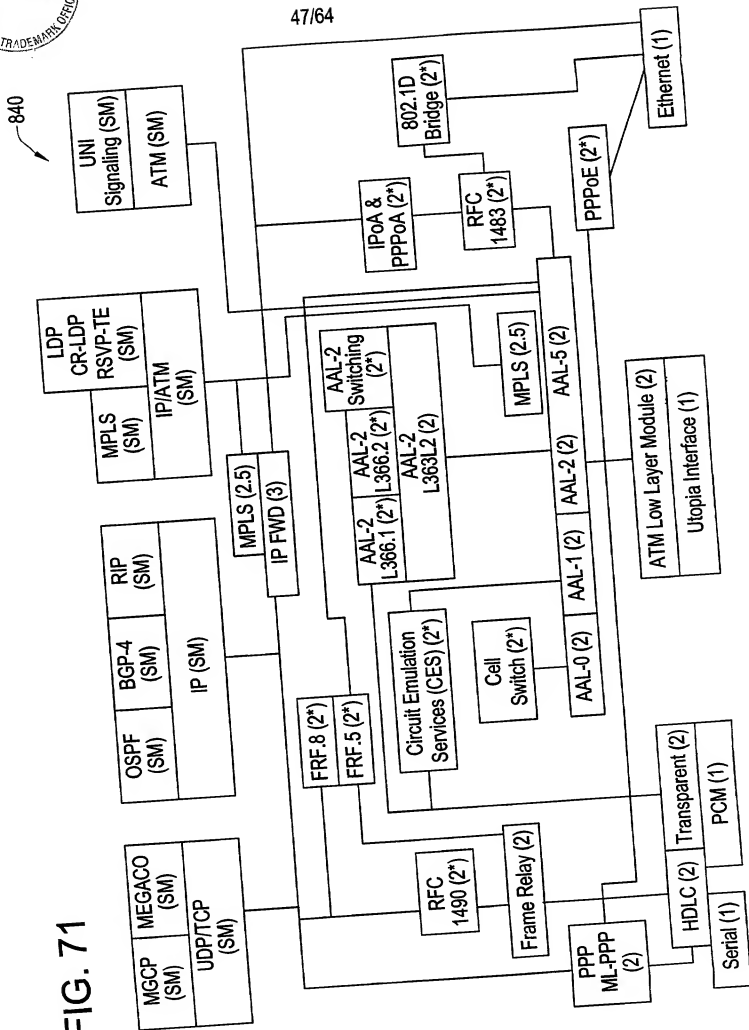


FIG. 72

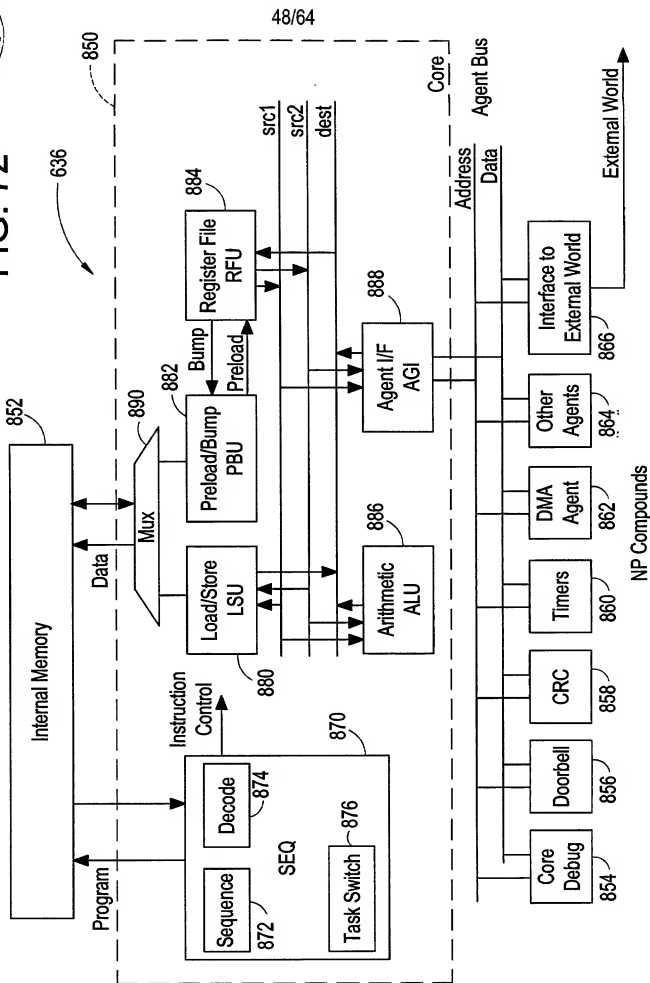




FIG. 73

900

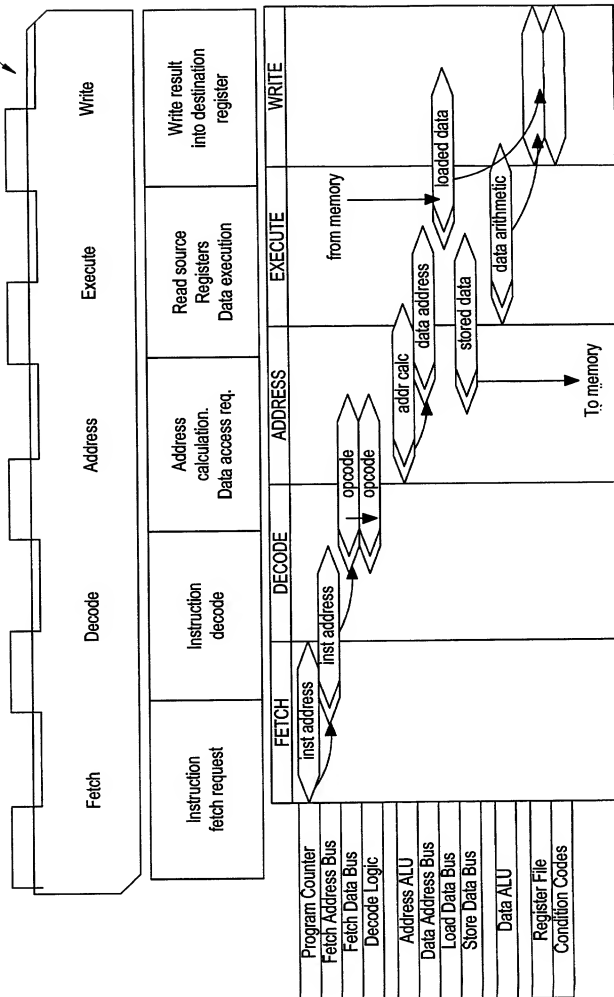


FIG. 74

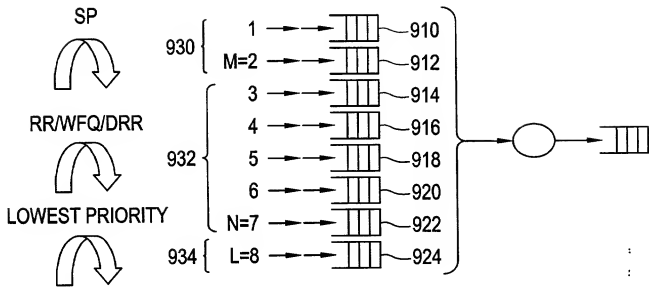


FIG. 75

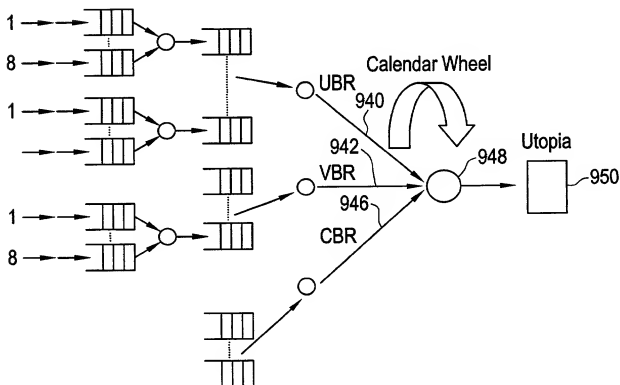


FIG. 76

960

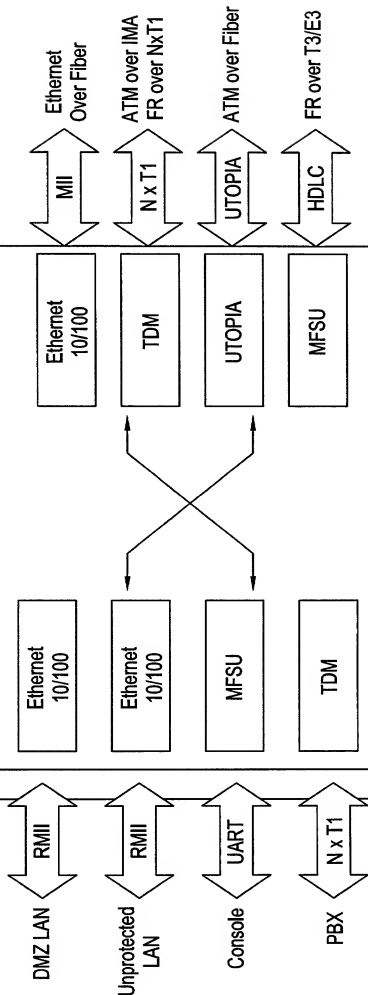


FIG. 77

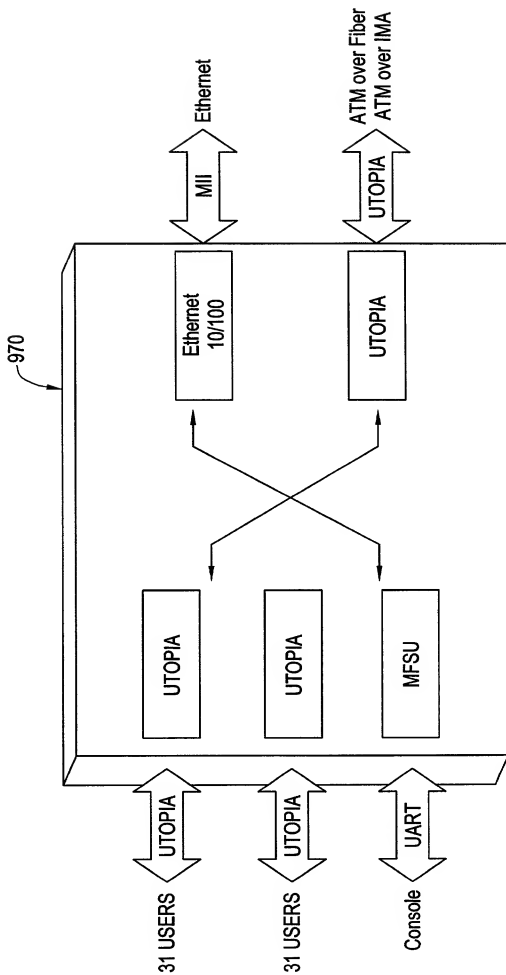


FIG. 78

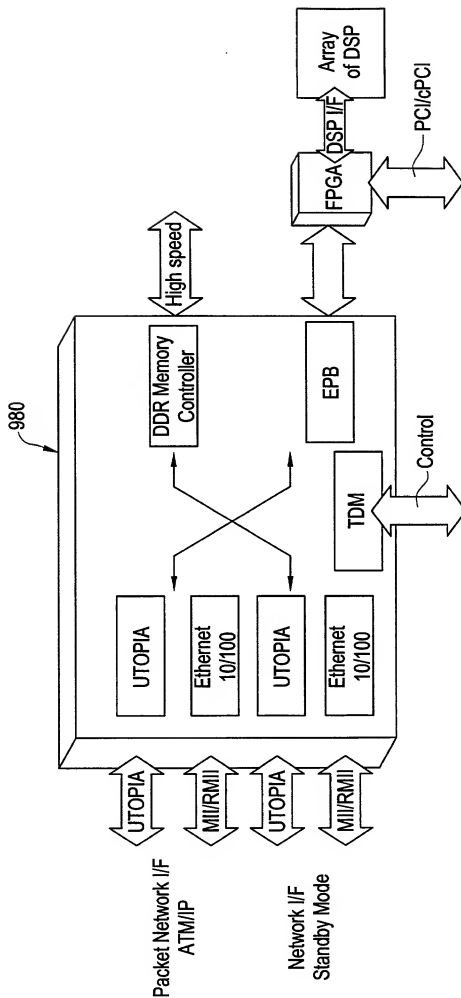


FIG. 79

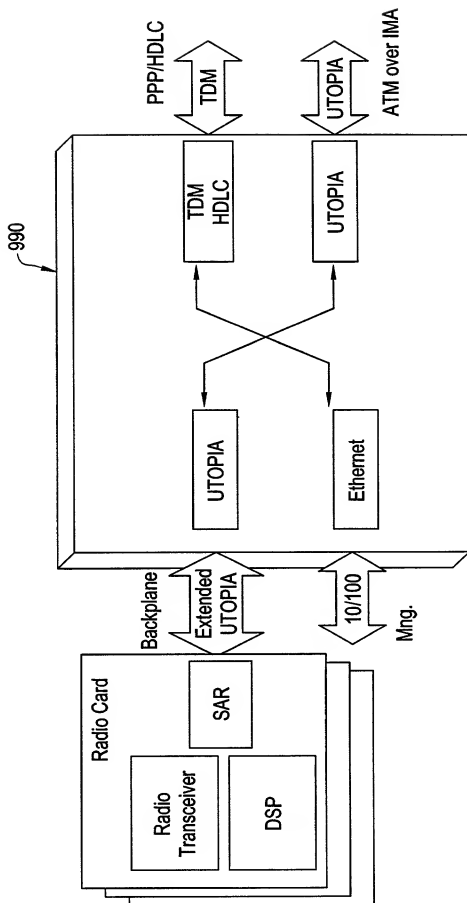


FIG. 80

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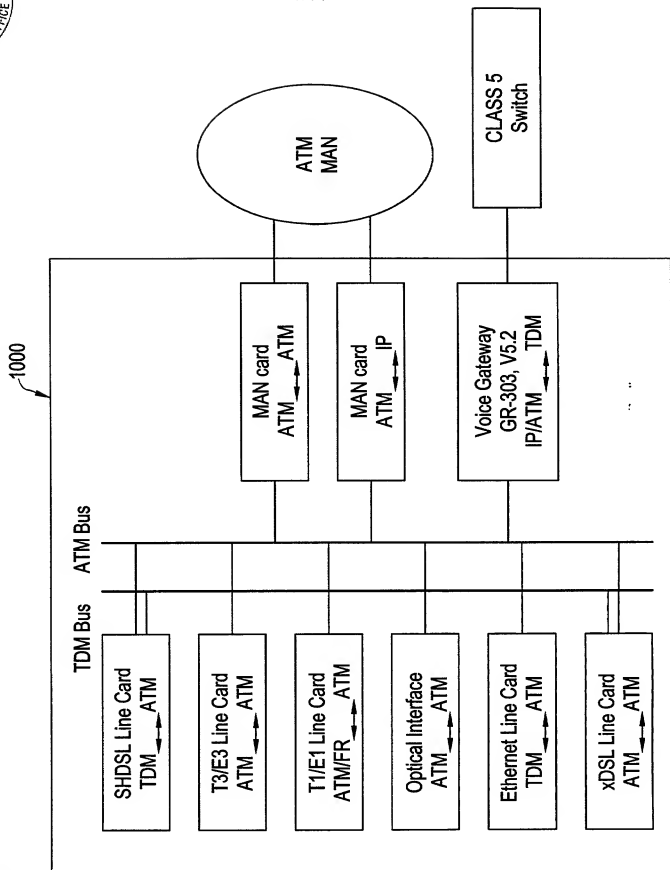


FIG. 81

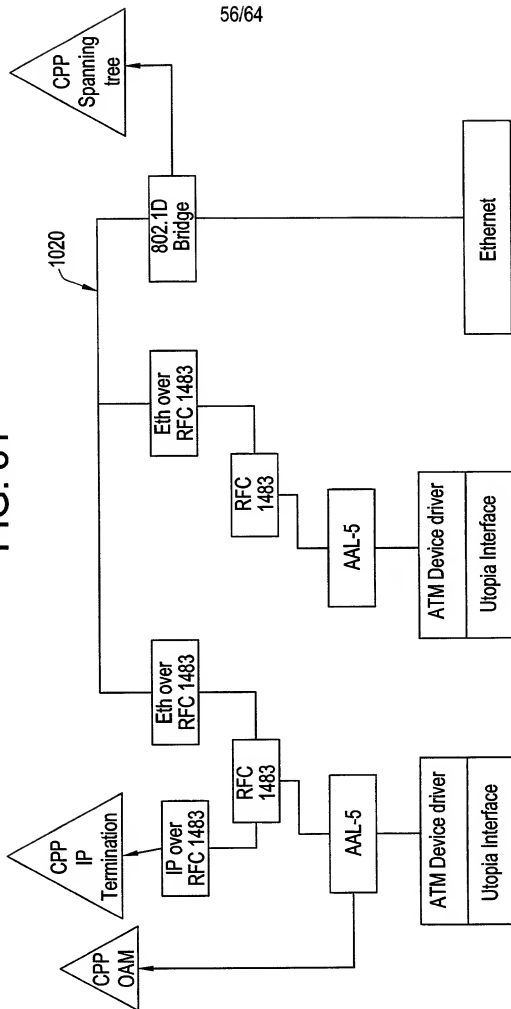




FIG. 82

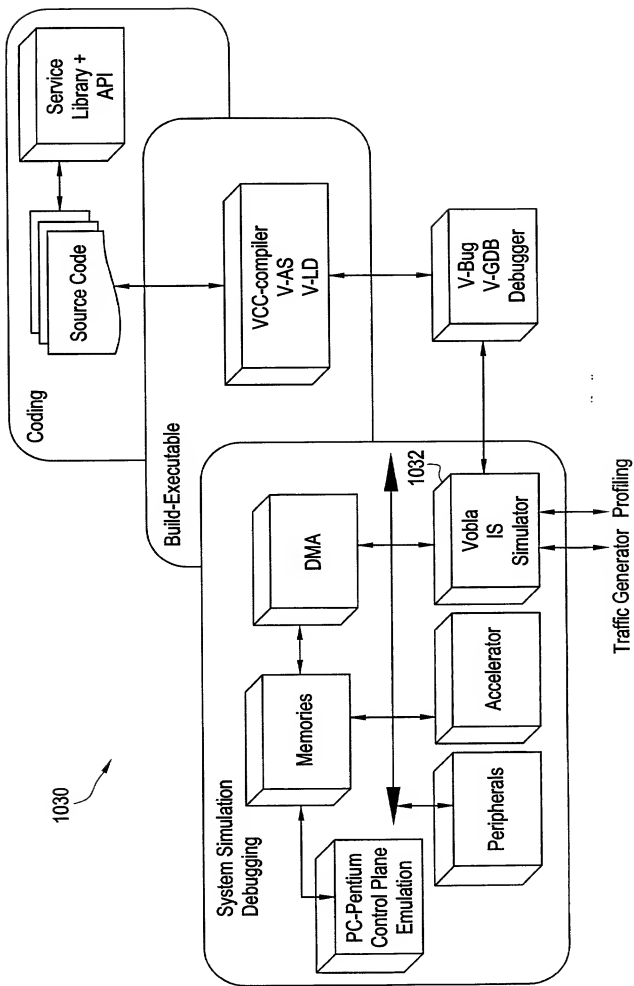


FIG. 83

1040

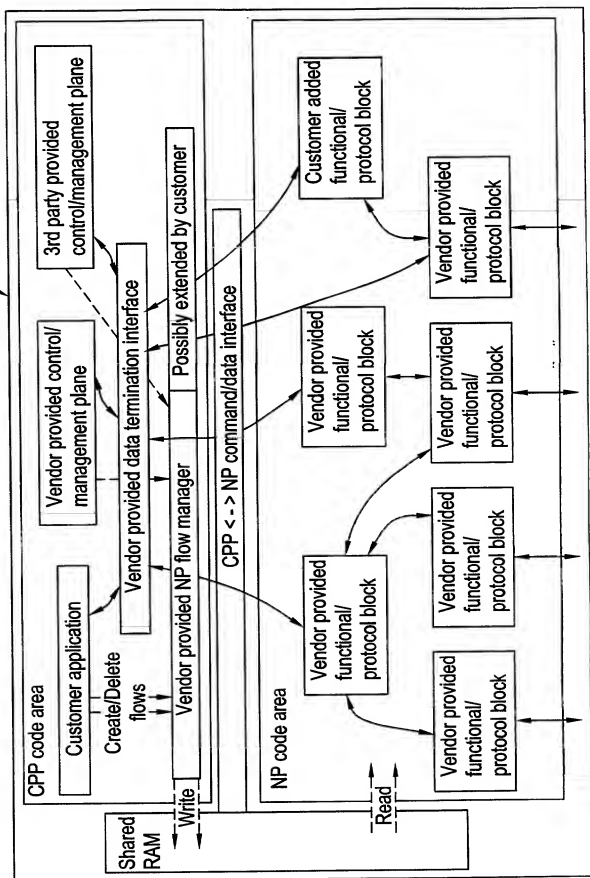


FIG. 84

1050

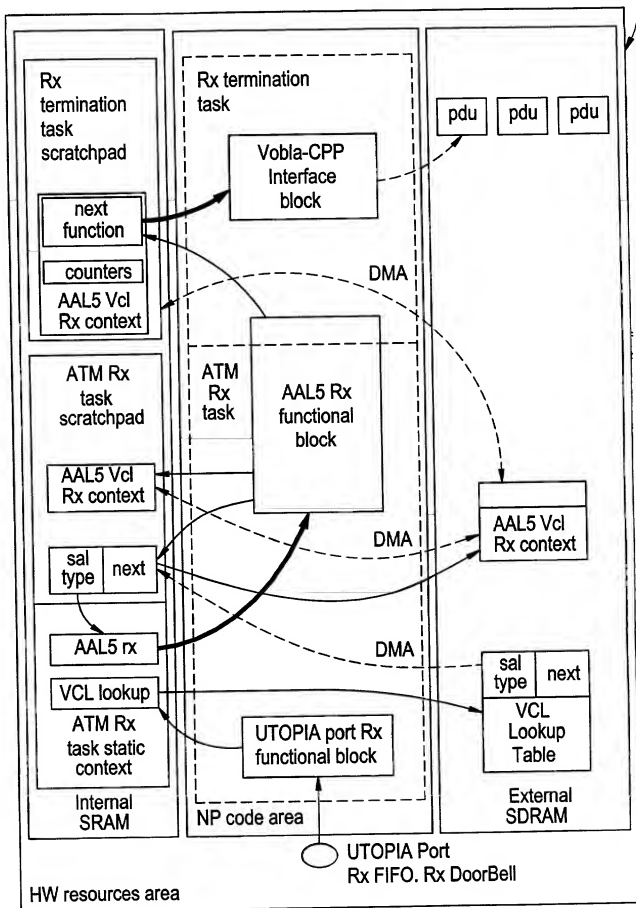


FIG. 85

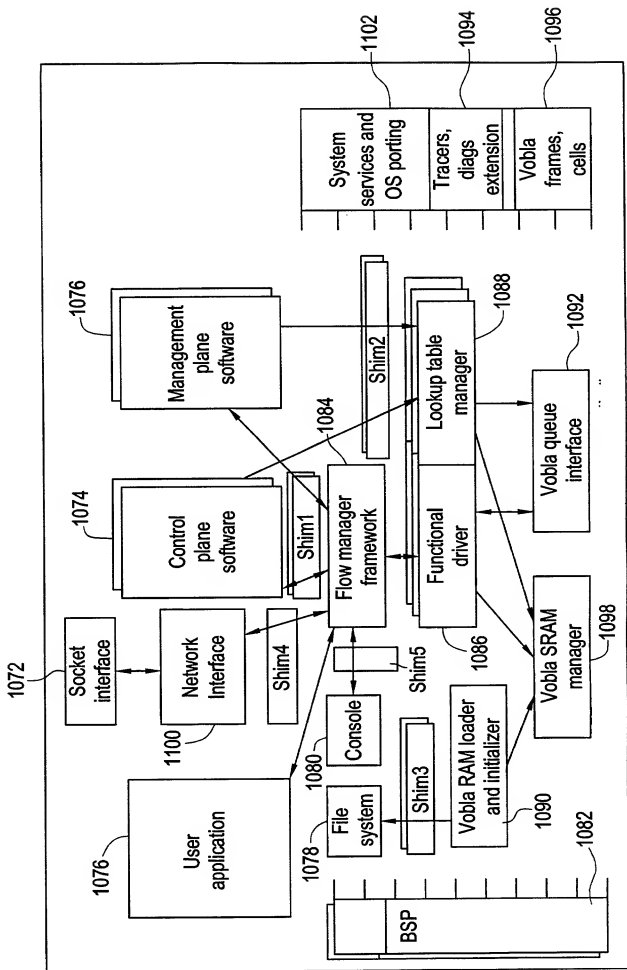
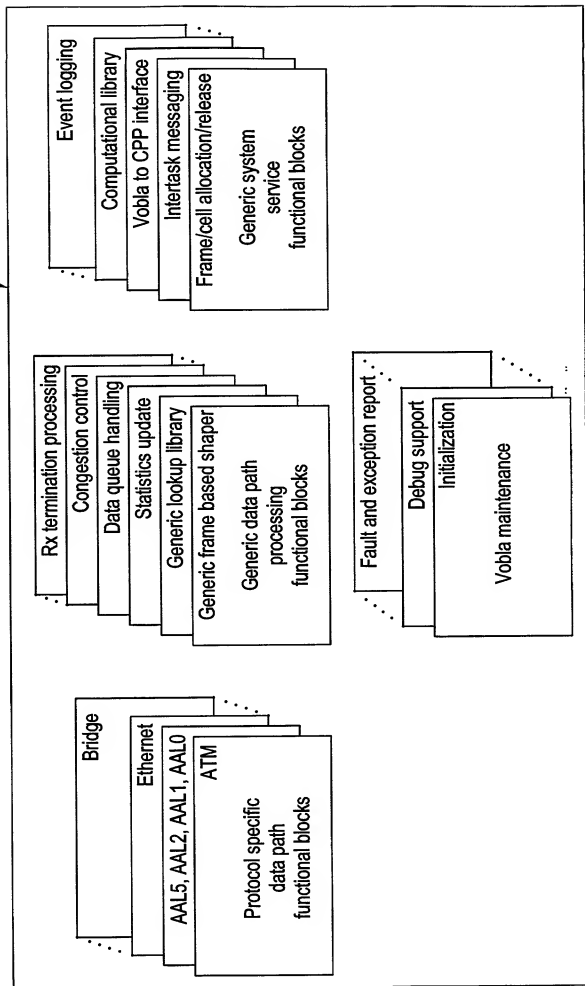


FIG. 86

1200





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# FIG. 87

PRIOR ART

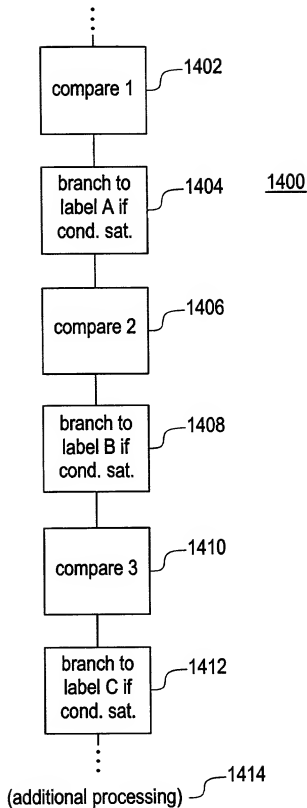


FIG. 87

FIG. 88

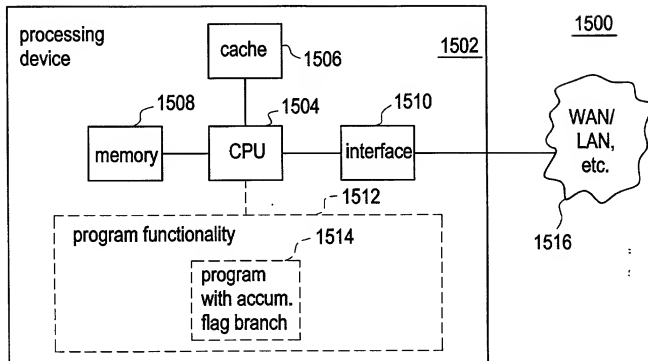


FIG. 89

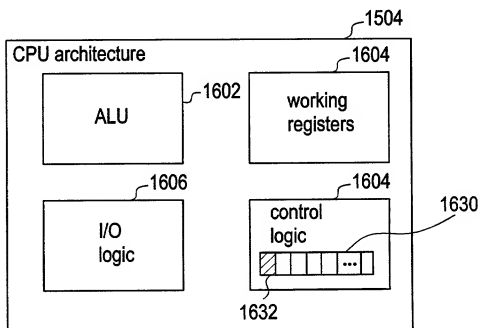


FIG. 90

